IN THE SPECIFICATION:

Please delete paragraph [0028] of the current specification.

Please replace paragraph [0160] with the following amended paragraph.

[0160] Figures 16a-16b illustrate a flow diagram of one embodiment for a process using multiply-add operations to perform bi-linear interpolation and motion compensation. In processing block 1601, a multiply-add operation is performed on the shuffled packed byte data 1612 stored in SRC1 and at least two area coefficients 1640 stored in SRC2 to generated Result 1610 including 16-bit sums of products. In processing block 1602, a multiply-add operation is performed on the second shuffled packed byte data 1622 stored in SRC1 and at least two more area coefficients 1650 stored in SRC2 to generated Result 1620 including 16-bit sums of products. Processing proceeds to processing block 1603 where a Result 1611 including 4n sums is generated by adding corresponding elements of the packed 16-bit sums of products of Result 1610 and Result 1620. In processing block 1604, rounding is optionally applied to the 4n sums of Result 1611 by adding rounding values ($s^2/2$) from packed data 1660 at the desired bit positions of the elements of Result 1611 to generate Result 1613. In processing block 1605, Result 1614 comprising 4n packed averages over an area (s^2) is computed from the 4n packed sums of Result 1613 by shifting the elements of Result 1613 by a shift count substantially equal to the log (base 2) of the area (i.e. $\log_2(s^2)$).